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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,918	12/01/2003	Ryosuke Usui	14225-034001 / F1030609US	3302

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EXAMINER	
LUHRS, MICHAEL K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/724,918	USUI ET AL.	
	Examiner	Art Unit	
	Michael K. Luhrs	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-12* is/are rejected.

7)☒ Claim(s) *3,8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Drawings

1. Figures 13A/B, and 14 and 15A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-7, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et. al. USPN 6,689,641 in view of Yew et. al. USPN 6,602,803.

Regarding claim 1, *forming conductive films that are laminated in multiple layers with interlayer insulating layers interposed in between*; Ohta et. al. teach laminated layers, line 12, column 10, first resin layer '7', line 24, column 10, second resin layer '9', lines 30-1, column 10; conductive layer 27, line 40, column 10, second conductive layer,'29', line 45-6, column 10 all in Fig. 1; *forming a conductive wiring layer by selective removal of the conductive film at a top surface*; Ohta et. al. teach top surface of conductive layer '31' is predetermined patterned, line 51, column 10; *forming through holes in the interlayer insulating layers and forming connection means in the through holes to electrically connect the conductive wiring layer with the conductive film at a rear surface*; Ohta et. al. teach through holes '14', lines 17-8, column 10, rear surface line 7, column 10.

Ohta et. al. are silent regarding *affixing and electrically connecting circuit element to the conductive wiring layer*; Ohta et. al. are silent on *irradiating plasma onto the conductive wiring layer, including the circuit element; and forming a resin layer so as to cover the circuit element.*

Yew et. al. teach *affixing and electrically connecting circuit element*, i.e. chip '10' in Fig. 1 to the conductive wiring layer, at pad '10b', lines 45-6, column 7; Yew et. al. teach *irradiating plasma onto the conductive wiring layer*, in line 67, column 8 to line 1 column 9, *conductive wiring layer* inherently at surface of chip finished through provision of BEOL structures, *including the circuit element;* includes chip '50' in Fig. 5 (or chip '10' in Fig. 1, line 2, column 9), *and* Yew et. al. teach *forming a resin layer so as to cover the circuit element,* as layer '12', lines 38-9, column 7, covers chip '10': all are steps to build the devices shown in Fig. 1, 3, 4 and 5. Since Yew et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Yew et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to *affixing and electrically connecting* chip '10' having pads '10b' in order to connect to substrate '11' having pads '13' (or to another chip in Fig. 5) and irradiating for the purpose of activating the resin in order to build the devices shown, with motivation of enhanced bonding.

Regarding claim 2, Ohta et. al. teach resin layer '11', line 15, column 10, wherein the conductive wiring layer is covered with resin while exposing locations that are to become pads, e.g. pads '32' of conductive layer '31', lines 53-4, column 10.

Regarding claim 4, Ohta et. al. teach *wherein connection means, comprising a plating film, are formed in the through holes to electrically connect the conductive wiring layer and the conductive film*, as seen in Fig. 1 showing throughholes: '14', (lines 17-8, column 10), e.g. plating '15', lines 20-1, column 10, comprised of plating (lines 4-6, column 13), connecting to '27' , (line 40, column 10), is a conductive film, (lines 11-12, column 13).

Regarding claim 5, Ohta et. al. is silent on oxygen. Yew et. al. teach oxygen, (as CF_4/O_2, in line 38, column 5) as a suitable plasma having an energy sufficient to break bonds (to enhance bonding adhesion). Since Yew et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Yew et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have

been obvious at the time the invention was made to a person having ordinary skill in the art to use the O_2 plasma for the purpose of enhanced bonding.

Regarding claim 7, Ohta et. al. silent on energy range. Yew et. al. teach energy sufficient to break the bonds (lines 37-38, column 5), is presumed within a range of 40eV to 100eV.

Regarding claim 9, Ohta et. al. teach *the conductive film is formed of a metal having copper as a principal material* as described in line 65, column 12.

Regarding claim 10, Ohta et. al. are silent of *wherein the circuit element is semiconductor element that is electrically connected via metal wires to the conductive wiring layer. The circuit element is semiconductor element* is taught by Yew, et. al. as chip '10', Fig. 1 *is electrically connected via metal wires to the conductive wiring layer* of substrate '11' by wiring '14'. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to connect a chip '10' as shown by Yew et. al. Fig. 1 to a substrate '11' having conductive wiring layer taught by Ohta et. al..

Regarding claim 11, Ohta et. al. are silent on a mounted chip in face down manner. Yew, et. al. show chip '10' having surface '10a' face is down against substrate '11' as shown in Fig. 1 for supplying the chip to a substrate of an IC package. Since Yew et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Yew et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the chip in a face down manner to the substrate, to permit the active area of the chip to be connected to the substrate of an IC package as shown by Yew et. al.'s Fig. 1.

Regarding claim 12, wherein the circuit element is electrically connected to the conductive wiring layer via soft solder or other solder material: the solder bump described by Ohta in line 30-31, column 15, is easily connected using lead/tin solder as described by Yew et. al. in lines 51-67, column 6. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to connect the conductive wiring of the substrate to the circuit element i.e. a chip, to permit the active area of the chip to be connected to the substrate of an IC package as shown by Yew et. al.'s Fig. 1.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et. al. and Yew et. al. as applied to claim 1 above, and further in view of Dery et. al. USPN 6,074,895.

Regarding claim 6, Ohta et. al. and Yew et. al. are silent on the inert, such as argon, neon, or helium. Dery et. al. teach *argon* and N_2O as an obvious variation of the plasma treatment (line 12-18, column 5). Since Yew et. al. and Ohta et. al. and Dery et. al. are all from the same field of endeavor, the purpose disclosed by Dery et. al. would have been recognized in the pertinent art of Ohta et. al. and Yew et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to generate the plasma with O_2 *or* the *argon* from microwave for the purpose of enhanced bonding.

Allowable Subject Matter

5. Claims 3, 8, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 3, *wherein in the step of irradiating plasma, the plasma is irradiated onto a top surface of the resin as well to roughen the top surface of the resin* ***while*** *a voltage, which is charged up in the resin, is released from the conductive wiring layer and via the conductive films: the* substrate connected to voltage for etching is known e.g. in rf etching, but *plasma is irradiated onto a top surface of the resin as well to roughen the top surface of the resin* ***while*** *a voltage, which is charged up in the resin, is released from the conductive wiring layer and via the conductive film* was not found.

Regarding claim 8, *wherein* ***after*** *the performing the plasma irradiation using oxygen gas, a plasma irradiation using an inert gas, such as argon, neon, or helium, is carried out*, was not found in Ohta et. al. or Yew et. al..

Regarding claim 13, the examiner would assert: that the substrate is prepared having the selectively removed conductive wiring at the rear surface, prior to its attachment to the chip, would thus occur *before* the plasma irradiation for activating the adhesive for said attachment.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Surface activation by irradiation with plasma: paragraph [0062] in PGPUB US 2002/0106831 and adhesion is made more firm by UV irradiation or plasma irradiation treatment in PGPUB US

2004/0006869. Satoh USPN 6,338,980 irradiates the resin for bump access fails to show the through hole to a rear conductive layer. Begle et. al. USPN 6,383,893 shows BEOL surface layering with copper and pads on a chip. Gaynes et. al. USPN 6,512,295 describe adhesive for heat dissipation. Kodnani et. al. USPN 6,596,559 face down flip-chip is well known.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael K. Luhrs

ANH PHUNG
PRIMARY EXAMINER